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1. A method of planarizing a structure on a semiconductor substrate, the method comprising:

depositing filler material over said horizontal surfaces to at least a thickness equal to said predetermined height so as to provide raised and lowered regions of filler material; and

2. The method of claim 1, wherein said filler material comprises non-conformal high density plasma oxide.

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1 4. The method of claim 1, further comprising covering said lowered
2 regions of filler material with a conformal coating, and wherein said selectively
3 removing comprises removing said coating from substantially all of said raised
4 regions, and etching said filler material on said raised regions, wherein during said
5 selectively removing adjacent sections of said upper and lower regions of filler
6 material are separated by at least a gap of exposed underlying material.

1 5. The method of claim 1, further comprising providing an oxide pad
2 on said semiconductor substrate and providing a nitride pad on said oxide pad,
3 wherein said raised and lowered regions are formed by masking regions of the
4 nitride pad and etching exposed areas of said nitride pad.

1 6. The method of claim 5, further comprising removing said oxide
2 pad and said nitride pad after selectively removing said raised regions of said filler
3 material.

1 7. The method of claim 1, wherein the selectively removing
2 comprises selectively etching only said raised regions of said filler material
3 without etching said lowered regions of said filler material.

8. A semiconductor substrate having a planarized trench region formed according to the method of claim 1.

9. A method for planarizing a trench region provided in a semiconductor substrate, the method comprising:
providing the semiconductor substrate with at least one trench region;
applying a filler material in the trench region and on the semiconductor substrate; and
removing only said filler material which is not provided in said trench region.

10. The method of claim 9, wherein said filler material comprises non-conformal high density plasma oxide.

11. The method of claim 9, wherein the removing comprises covering the trench region with a mask and etching said filler material from regions which are not protected by said mask.

12. The method of claim 9, further comprising covering said trench region with a conformal coating, and wherein said removing comprises removing

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3 said coating from substantially all non-trench regions and etching said filler
4 material on the non-trench regions.

1 13. The method of claim 9, further comprising providing an oxide pad
2 on said semiconductor substrate and providing a nitride pad on said oxide pad,
3 wherein said at least one trench region is formed by masking regions of said
4 nitride pad and etching exposed areas of said nitride pad.

1 14. The method of claim 9, further comprising removing said oxide
2 pad and said nitride pad after removing the filler material which is not provided in
3 the trench region, wherein adjacent sections of said trench regions and non-trench
4 regions of filler material are separated by at least a gap of exposed underlying
5 material.

1 15. A semiconductor substrate having a planarized trench region
2 formed according to the method of claim 9.

1 16. A method of forming a planarized structure on a semiconductor
2 substrate, the method comprising:
3 providing the semiconductor substrate with a trench region and
4 non-trench regions;

5 depositing filler material on said trench region and said non-trench
6 regions, said filler material filling said trench region to a predetermined height;
7 and

8 removing said filler material from said non-trench regions while
9 allowing said filler material in said trench region to remain filled to the
10 predetermined height.

1 17. The method of claim 16, wherein said filler material comprises
2 non-conformal high density plasma oxide.

1 18. The method of claim 16, wherein adjacent sections of said trench
2 region and non-trench region of filler material are separated by at least a gap of
3 exposed underlying material and the removing comprises covering said trench
4 regions of filler material with a mask and etching said filler material on said
5 non-trench regions which are not protected by said mask.

1 19. The method of claim 16, wherein the removing comprises covering
2 said trench regions of filler material with a conformal coating, and wherein said
3 removing comprises removing said coating from substantially all of said non-
4 trench regions, and etching said filler material on said non-trench regions, wherein
5 during the removing adjacent sections of said trench region and non-trench region

6 of filler material are separated by at least a gap of exposed underlying material.

1 20. The method of claim 16, further comprising providing an oxide
2 pad on said semiconductor substrate and providing a nitride pad on said oxide
3 pad, wherein said trench region and the non-trench regions are formed by masking
4 regions of said nitride pad and etching exposed areas of said nitride pad.

1 21. The method of claim 20, further comprising removing said oxide
2 pad and said nitride pad after removing said filler material on the non-trench
3 regions.

1 22. The method of claim 16, wherein the removing comprises
2 selectively etching said filler material on the non-trench regions without etching
3 said filler material on the trench regions.

23. A semiconductor substrate having a planarized structure formed
according to the method of claim 16.

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